Design and FPGA Implementation of On-Chip Network Topology with Port Addressing Scheme for Permutation Network

[1]Umadevi R., [2]Sandhya Rani M.H., [3]B.N. Shobha

[1]Student, M Tech, [2]HOD, Dept. of ECE, [3]Assoc Prof, Dept. of ECE
[1]VLSI Design and ES, [2,3] SCE Bangalore, VTU, [1,2,3] Dept. of ECE, SCE Bangalore, VTU

Abstract: **The communication mechanism is employed in system on a single chip is an important contribution to their overall performance. The data bus based mechanism is applied in many areas of real time applications of Socs realizing on FPGA due to its flexibility and simplification in designing tool. It challenging task in a network-on-chip to design an on-chip switch /router to support (hard) guaranteed throughput under very tight on-chip constraints of power, timing, area and time-to-market. This paper presents an on-chip network to support traffic permutation in multiprocessor SoC applications. The proposed network employs a pipelined circuit switching approach combined with a path-setup scheme under a multistage network topology. The circuit-switching approach offers a guarantee of permuted data and its compact overhead enables the benefit of stacking multiple networks with saving power and area. The proposed design is develop using Xilinx 9.1ISE, Simulated on modelsim 6.3f and implemented on Spartan 3 device.**

Keywords: **Multistage Interconnection Network, Network-on-chip, Traffic permutation network, Circuit Switching, Dynamic path setup scheme, and system- on-chip and Network topology.**

I.   INTRODUCTION

A trend of multiprocessor system-on-chip (MPSOC) design interconnected with on-chip networks is currently emerging for applications of parallel processing, scientific computing ,and so on [1]-[6]. Permutation traffic , a traffic pattern in which each inputs sends traffic to exactly one output and each output receives traffic from exactly one input, is one of the important traffic classes exhibited from on-chip multiprocessing applications[7],[8]. Standard permutations of traffic occur in general-purpose MPSOCs, for example, polynomial, sorting and fast Fourier transform (FFT) computations because shuffled permutation, whereas matrix transposes or corner-turn operations exhibit transpose permutation [6]. Recently, application- specific MPSOCs targeting flexible Turbo/LPDC decoding have been developed, and they exhibit arbitrary and concurrent traffic permutations due to multi-mode and multi-standard feature [3]-[5]. In addition, many of the MPSOC applications (e.g., Turbo/LDPC decoding [3]-[5]) compute in real-time, therefore, guaranteeing throughput i.e., data lossless, predictable latency, guaranteed bandwidth, and in-order delivery is critical for such permutation. Most on-chip networks in practice are general-purpose and use routing algorithms such as dimension-ordered routing and minimal adaptive routing. To support permutation traffic patterns, on-chip permutation networks using application-aware routings are needed to achieve better performance compared to the general-purpose networks [8].These application aware routings are configured before running the applications and can be implemented as source routing or distributed routing. However, such application-aware routings cannot efficiently handle the dynamic changes of a permutation pattern, which is exhibited in many of the application phases [8]. The difficulty lies in the design effort to compute the routing to support the permutation changes in runtime, as well as to guarantee [9] the permutated traffics. This becomes a great challenge when these permutation networks need to be implemented under very limited on-chip power and area overhead.

II.   APPROACHES USED

This approach mainly depends on three factors   they are Switching techniques, topology and routing algorithm

A. Switching techniques:

In large networks there might be multiple paths linking sender and receiver. Information may be switched as it travels through various communication channels. There are three typical switching techniques available techniques for digital traffic. They are: Circuit switching, Message switching and Packet switching

(i) Circuit switching:

Circuit switching is a technique that directly connects the sender and receiver in an unbroken path. Telephone switching equipment, for example, establishers a path that connects the caller's telephone to the receiver's telephone by making a physical connection. With this type of switching technique, once a connection

is established, a dedicated path exists between both ends until the connection is terminated. Routing decisions must be made when the circuit is first established, but there no decisions made after that time.

(ii) Message switching:

With message switching there is no need to establish a dedicated path between two stations. When a station sends a message, the destination address is appended to the message. The message is then transmitted through the network, in its entirety, from node to node. Each node receives the entire message, stores it in its entirety on disk, and then transmits the message to next node (fig1).this type of network is called a store-and-forward network.
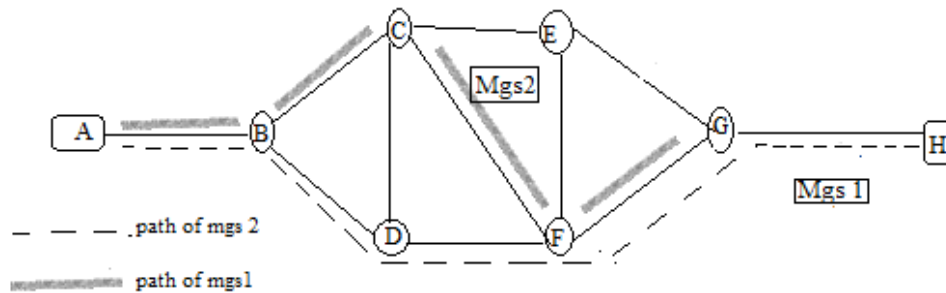
Fig 1: message switching [2]

(iii)Packet switching:

There are two methods of packet switching: Datagram and virtual circuit. In both packet switching methods, a message is broken into small parts, called packets. Each packet is tagged with appropriate source and destination addresses. Since packets have a strictly defined maximum length, they can be stored in main memory instead of disk (fig 2). Therefore access delay and cost are minimizing. Also the transmission speeds, between nodes, are optimized. With current technology, packets are generally accepted onto the network on a first-come, first-served basis. If the network becomes overloaded, packets are delayed or discarded ("dropped")
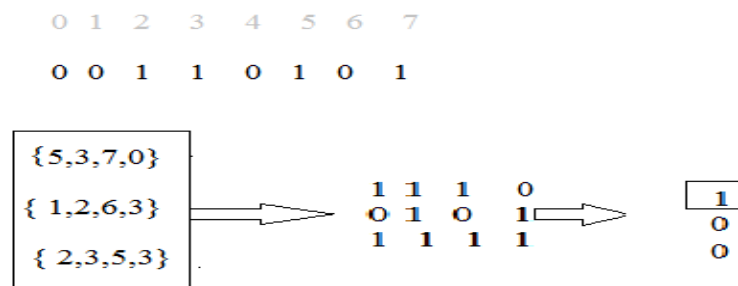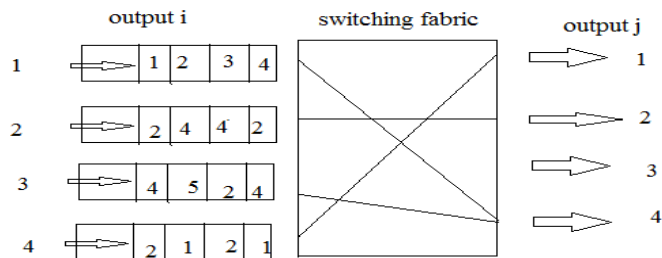
Fig 2: packet switching [2]

B. Topology:

The topology used is "3 –stage clos". It provides 0.13µm CMOS technology with low power consumption packet data transmission .this topology provides better throughput with less area requirements (fig 3)

Fig 3: packet switching with 3-stage clos topology [2]

C. Routing algorithm:

Routing is the process that a router uses to forward packets toward the destination network. A Router makes decisions based upon the destination IP address of a packet. In order to make the correct decisions, routers must learn the direction to remote networks. Two types of routing are used: static and dynamic routing [1]. When routers use dynamic routing, this information is learned from other routers. When static routing is used, a network administrator configures information about remote network manually.

III.   METHODOLOGY

The system design includes software design and hardware implementation, on-chip network topology, dynamic path-setup scheme.

A. system-on-chip:

System-on-chip is an integrated circuit (IC) that integrates all components of a computer or other electronic system into a single chip. It contain digital, analog, mixed-signal, often radio-frequency functions every on a single chip substrate system-on-chip on a VLSI chip that all needed analog as well as digital circuits, processor and software. The demands on computer chips and processors these days are staggering. Even the simplest computer is required to complete complex tasks simultaneously. The benefits of SoC are self-evident everything needed to run the computer is contained in that one chip-the smaller and better. This includes the computer's operating system, electronic functions, memory of all variety, timers, interfaces like USB and Fire-wire, Voltage regulators, timers, microprocessors and basic function software applications. The chip has all that is required to run still detailed computer functions.

SoC= Chip+ software +Integration.

B. Network-on-chip:

Network on chip is a communication subsystem on integrated methods to on-chip communication and bring remarkable improvements over conventional bus and crossbar interconnections. NoC improves the scalability of SoCs, and the power efficiency of complicated SoCs compared to other designs. Network on chip is an emerging for communications within large VLSI systems implemented on a single silicon chip. As the number of IP modules in system-on-chip (SoCs) increases, bus-based interconnection architectures may prevent these systems to meet the performance required by many applications. For systems with demanding parallel communication requirements buses may not provide the required bandwidth, latency and power consumption. A solution for such a communication bottleneck is the use of an embedded switching network, called network-on-chip, to interconnect the IP modules in SoCs. In addition, NoCs have an inherent redundancy that helps tolerate faults and deal with communication bottlenecks. This enables the SoCs designer to find appropriate solutions for different system characteristics and constraints.

C. Clos Network:

Clos network is a multistage network topology is a multistage network topology which is used in switching technique for data transfer in three stages, and also it has sixteen inputs and outputs , each path is select dynamically according to the

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input given. The main advantage of network is that connection between a large number of input and output ports can be made by using only small-sized switches.
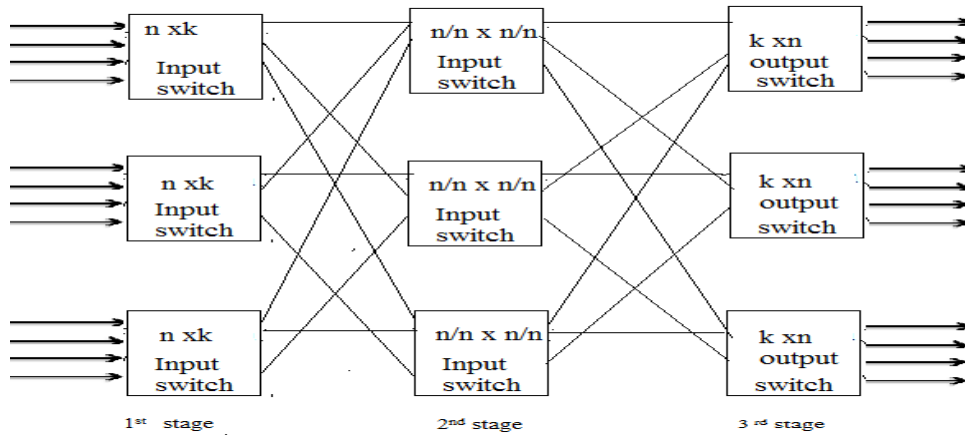

Fig 4: 3 stage clos network [3]

In figure 4, n represent the number of sources which feed into each of the m ingress stage crossbar switches. There is exactly one connection between each ingress stage switch and each middle stage switch. And each middle stage switch is connected exactly once to each egress stage switch. Clos network is non-blocking when m>n-1, ingress/egress stage has r n x m switches, middle stage has m r x r switches, and each switch at ingress/egress stage connects to all m middle switches. This network has a rearrangeable property that can realize all possible permutations between its input and outputs. The variety of the three stage clos network with a modest number of middle–stage switches is to minimize implementation cost, whereas it still has a rearrange able property for the network.

IV.   EXISTING COMMON SWITCH ARCHITECTURE FOR CLOS NETWORK

This existing network works based the common switch architecture. This common architecture shown in figure with only difference being in the probe routing algorithms. This common architecture has components input control (Ics), output controls (Ocs), an arbiter, and a Crossbar. The arbiter has functions first, cross connecting the Ans-outs and the Ics through the grant bus, and second, as a referee for the requests from the   Ics. When an incoming probe arrives at an input, the corresponding IC observes the output status through the status bus and requests the arbiter to grant it acess to corresponding Ans-out with the IC through the grant bus with its first function. With the second function, the arbiter, based on a pre-defined priority rule, resolves contention when several Ics request the same free output. After this resolution, only one IC is accepted, whereas the rest are answered as facing a blocked link. The IC is implemented with finite –state machine (FSM).
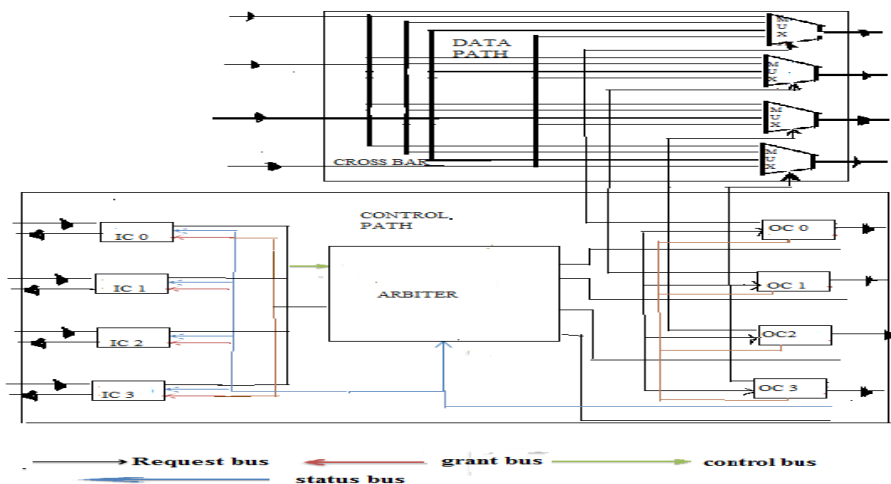

Fig 5: common switch architecture for clos network [1]

V.   PROPOSED ON-CHIP NETWORK DESIGN

The figure6 shows the architecture of proposed network.This is architecture consists of in,out, arbiter and crossbar and decoder. In figure6 shows the d_{in} and d_{out} denotes the input and output of the switch.
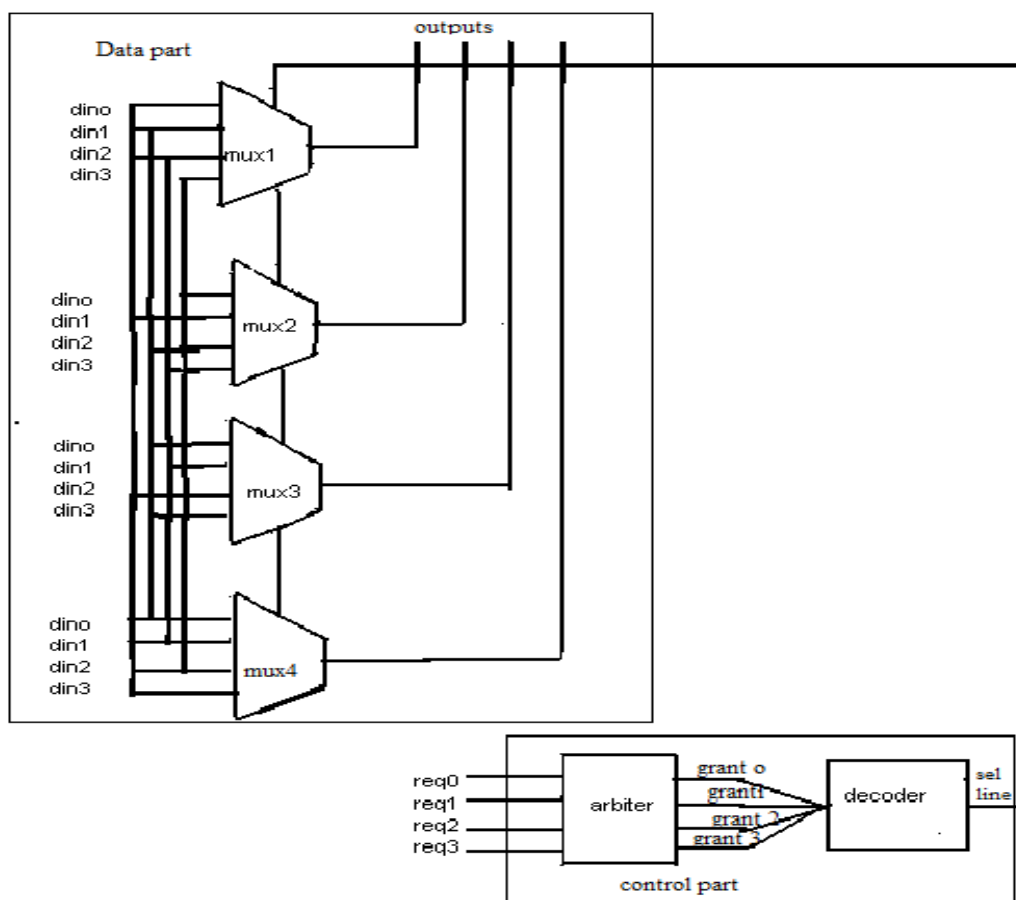

Fig 6: Shows single switch architecture for proposed network

This architecture can be divded into two function groups the data path includes crossbar to support a direct source synchronous data. Crossbar is switch connecting multiple inputs to multiple outputs in a matrix manner. This cross bar switch designed by mux tree architecture .mimimum four muxes are using to generated the ouputs. The control parts includes in ,out ,arbiter and decoder.The arbiter consist of no of status register the operation of arbiter is it sloves the contention problem. And it acknoweldge whether the link is free or busy i,e denote by status register. This arbiter will implemented by using FSM .for example if a request is arrived to any one of the input say req1 then arbiter will grant and it will move on to idle state.if many request arrive at the same time it will perform comparsion and according to the proporty it will grant the output. Arbiter gives the output to the decoder ,decoder gives the select output which gives to the crossbar which acts as the select line for the crossbar.According to the value of the select line in the cross bar the particular mux will get selected and gives the output.

A. PROPOSED ON-CHIP NETWORK   TOPOLOGY:

Clos network,a family of multistage networks, is applied to bulid scalable commercial multiprocessor with thousands of nodes in macro systems.A typical three –stage clos network is defined as C(n,m,p), where n represents the number of inputs in each of P first-stage switches and m is number of second stage switches. In order to support a parellelism degree of 16 as in most practical MPSoCs,[3] the proposed to use C(4,4,4)as a topology for the designed network as in the figure 7. On-chip network topology with port adderssing secheme as shown in the figure 7, Phi-Hung Pham et al [1]. In this network topology has 16-bit data path-setup scheme is the key point of the proposed design to support a runtime path arrangement when the permutation is changed. Each path system, which starts from an input to find a path leading to its corresponding output.
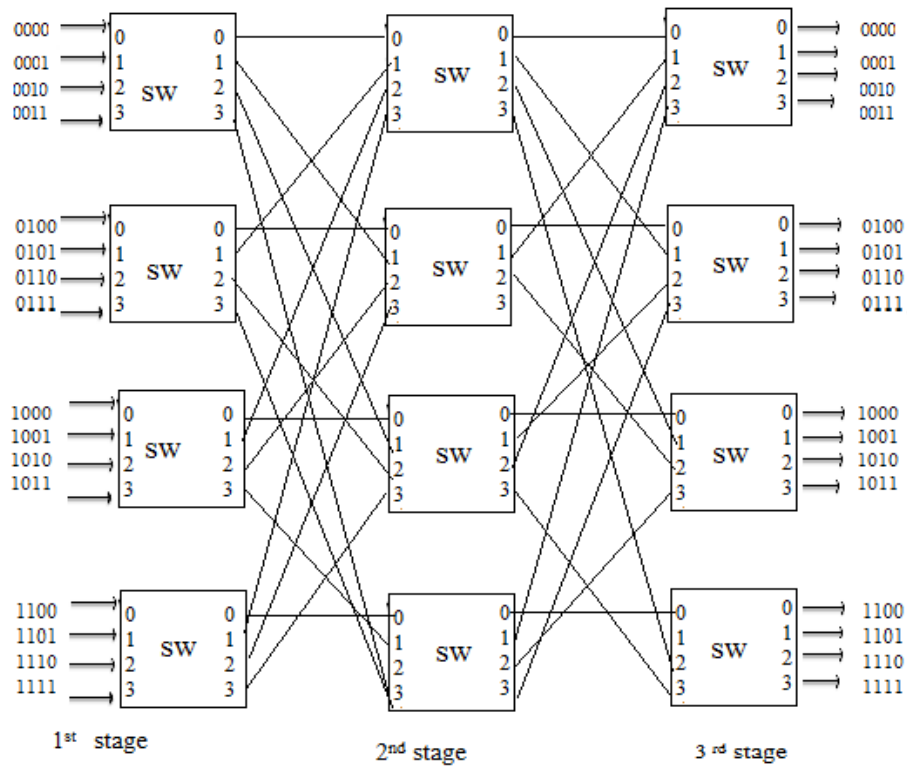
Fig 7: proposed on-chip network topology with port addressing scheme [1]

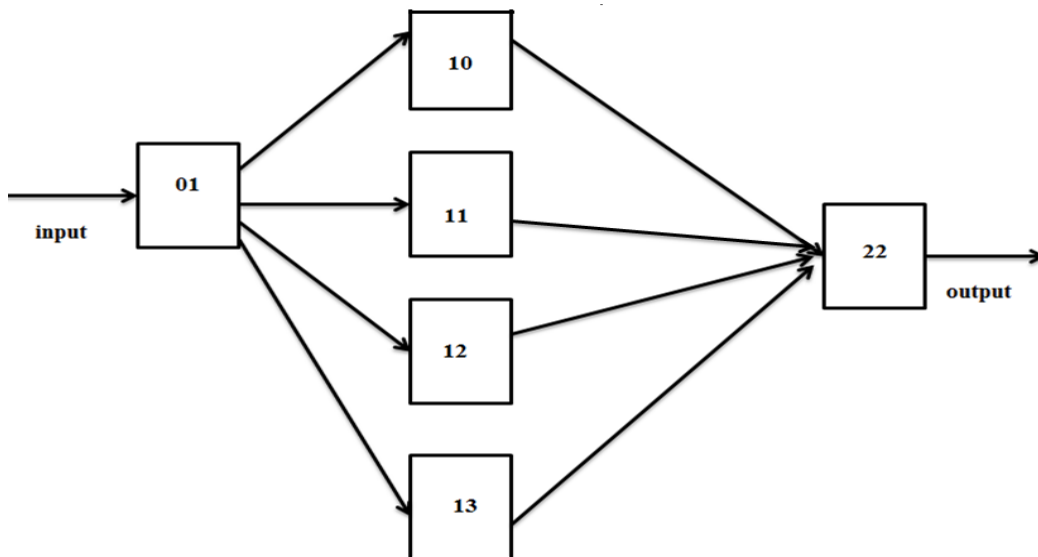**B. SWITCH-BY-SWITCH INTERCONNECTION AND PATH-DIVERSITY CAPACITY FOR THE PROPOSED NETWORK:**

Fig 8: switch-by-switch interconnection and path- diversity capacity [1]

In figure 8 shows how the path setup works to find an available path by using the set of path diversity shown in the figure 8. It is assumed that a link from source e.g., an input of switch 01 is trying to set up a path to target destination e.g., an available output of switch 22. First, the link will non-repetitively try paths through the second-stage switches in the order of 10—11—12—13. Assuming that link 01-10 is available, the probe first tries this link and then arrives at switch 10. If link 10—22 is available, the probe arrives at switch 22 and meets the target output. If link 10—22 is blocked, and will move back to switch 01 and link 01-10 is released. From switch 01, the link can try the reset of idle links leading to the second stage switches in the same manner.
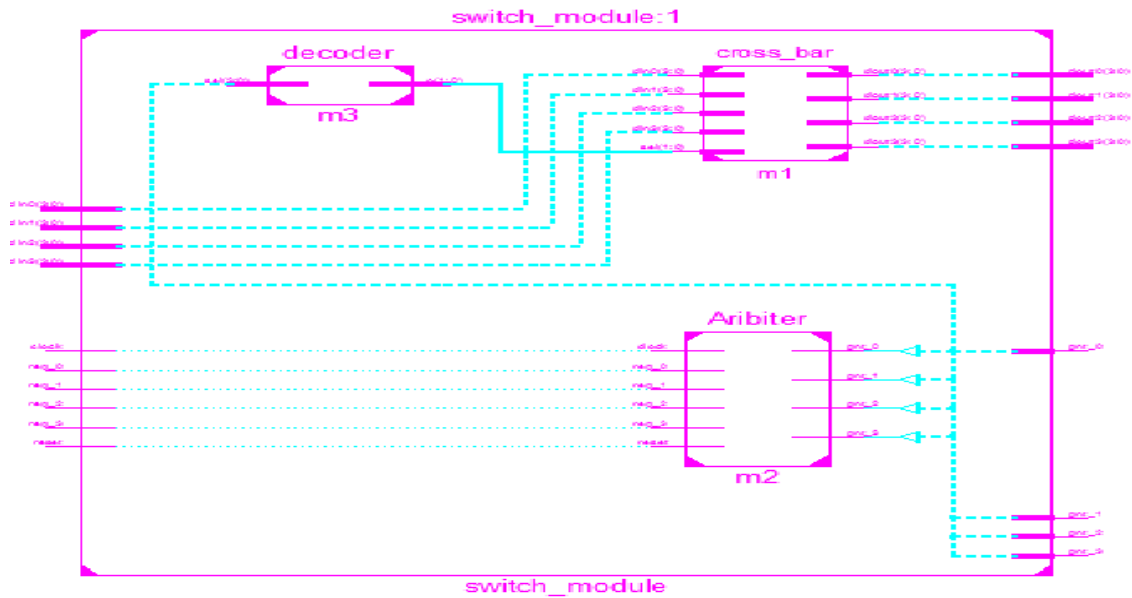
VI. IMPLEMENATION AND RESULTS

Fig 9: RTL Schematic view of single switch architecture for a proposed network

This architecture consists of in, out, arbiter, crossbar and decoder. The in and out denotes the input and output pins of the switch. The arbiter is used to connect in and ans-out with help of the grant bus. It is only through the arbiter the switch inputs request the output link. The status register are used to backtrack the source in order to send acknowledgement upon reception of data by the destination and denotes whether the link is free or busy. Arbiter also solves the contention problem by serving the input which requested earlier when several input pins request the same output pin. In this architecture the FSM is implemented only in the arbiter.
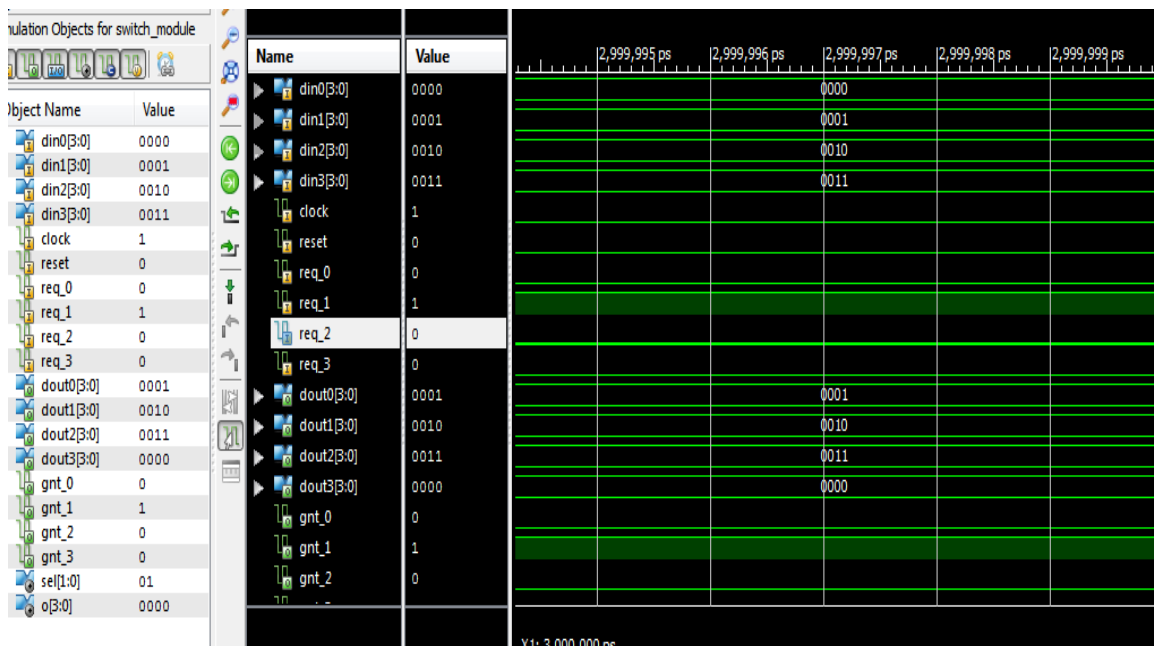
A. SIMULATION WAVEFORM FOR SWITCH ARCHITECTURE:

Fig 10: shows the Simulation waveform for switch architecture

The figure 10 shows the wave form for common switch architecture for single switch for port addressing secheme for permutation network .They are 4 inputs to the arbiter they are req 0 to req 3 and output they are grant0 to grant3 . If a

request is arrvied to any one of the input say for example req 1 then arbiter will grant and it will move on to the next state. If none of the request available it will move on the the idle state.If many request arrive at the same time it will perform comparsion and according to propority it will grant the output .If the input to din1=0001 and select line s0 and s1=01 then the output will dout=0001 , so particular line will connect to the output. According to value of select line in the crossbar, the particular mux will get selected.

B. SIMULATION WAVEFORM FOR ARBITER:

Whenever inputs have to be applied ,clock should be asserted by the clock (do not forcing the value) and for the first cycle reset should be forced to 1 and next cycles we can apply 0 and soon whenever the req bus to 1 is applied, it will grant it for next cycle ,then the acknowledgement will be sent. Then for the next cycle it will observe the status of request bus and responds to next grant bus by asserting grant to 1.when all request are raised to 1.like this the arbiter is going to provide the grant, based on their priority.

Fig10: simulation waveform for arbiter when all are request high

## C. RTL SECHEMATIC VIEW OF PROPOSED NETWORK:
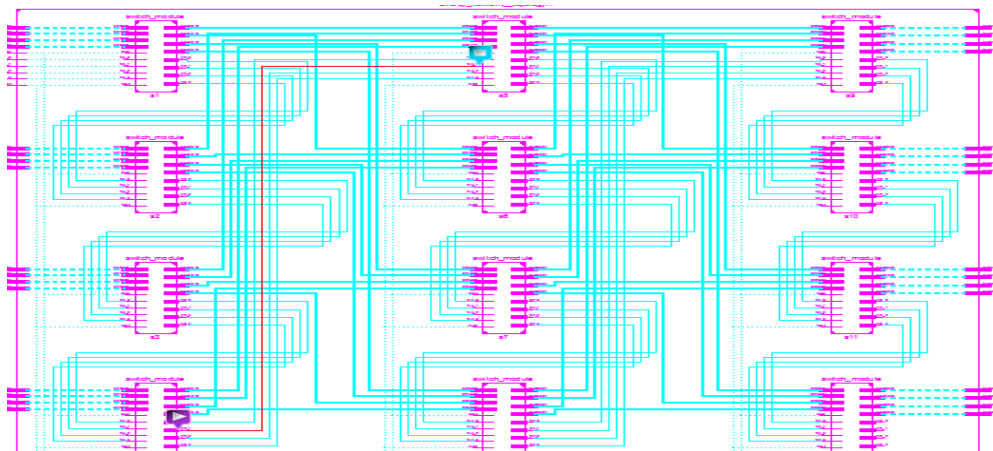
Fig 11: RTL schematic view for proposed network

In this figure 11 shows the network topology has 16-bit data with path-setup scheme is the key point of the proposed design to support a path arrangement when the permutation is changed. Each path system, which starts from an input to find a path leading to its corresponding output.

D. SIMULATION WAVEFORM FOR PROPOSED NETWORK:
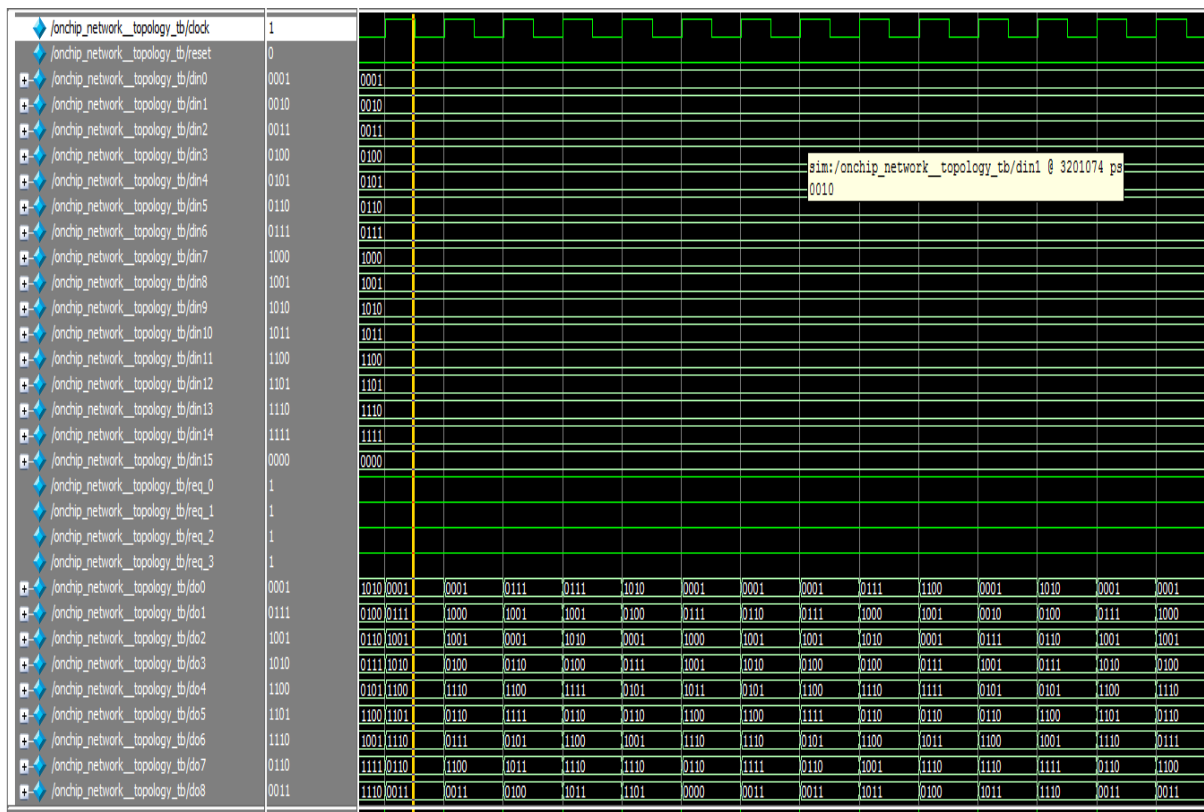
Fig 12: shows the simulation waveform for proposed network

The figure 12 shows the simulation waveform for proposed netwok design consist 16- bit data to the network it support a path arrangement when the permutation is changed. Each path system, which starts from an input to find a path leading to its corresponding output.
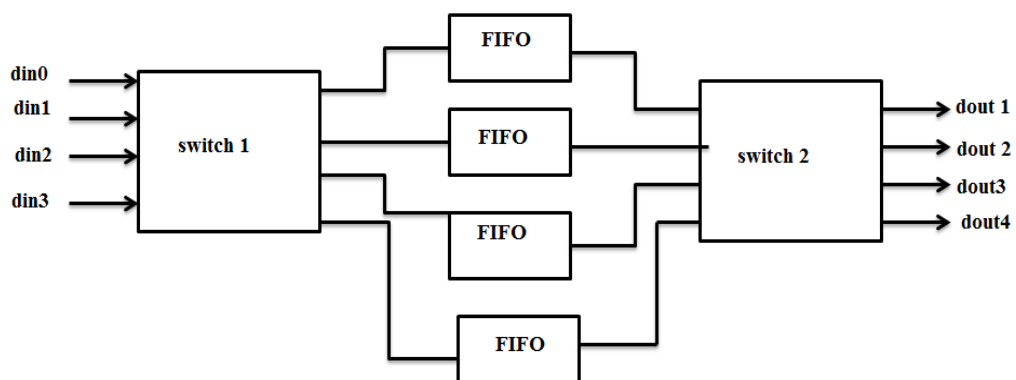
VII.   SWITCH BASED WRAPPER CIRCUIT PROPOSED NETWORK

Fig 13: shows the switch based wrapper circuit for proposed network

 In figure 13 shows the FIFO based test wrappers interfaced with the proposed on-chip network is used, but here we using only 2x2 switches network to test end –to-end synchronous data transfer scheme. The 32Wx16 bit FIFO is used to log the test data transmitted from source to destination, and support the source- synchronous transfer scheme.Fig13 details the source synchronous transfer scheme, in which one wire of the data path is dedicated for source clock transmission.

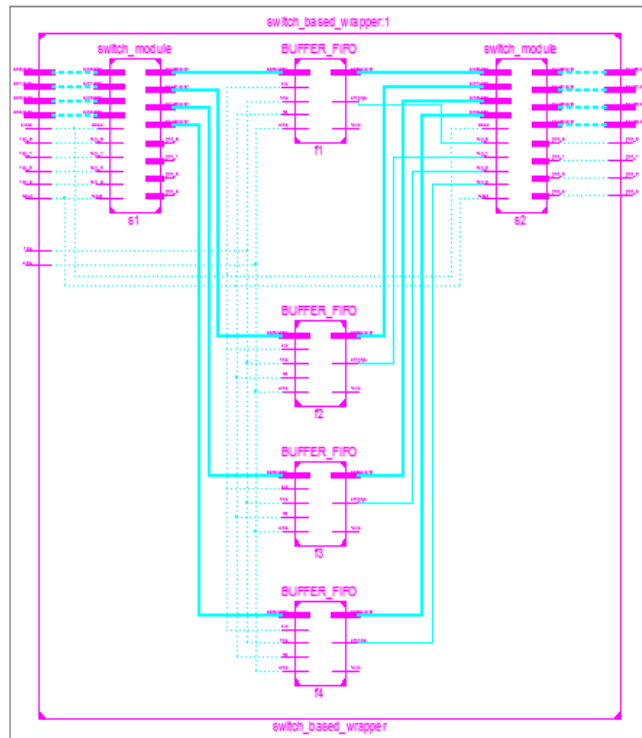## 1. RTL SCHEMATIC VIEW OF SWITCH BASED WRAPPER CIRCUIT FOR PROPOSED NETWORK:

Fig14. RTL Schematic View of Switch Based Wrapper Circuit for Proposed Network

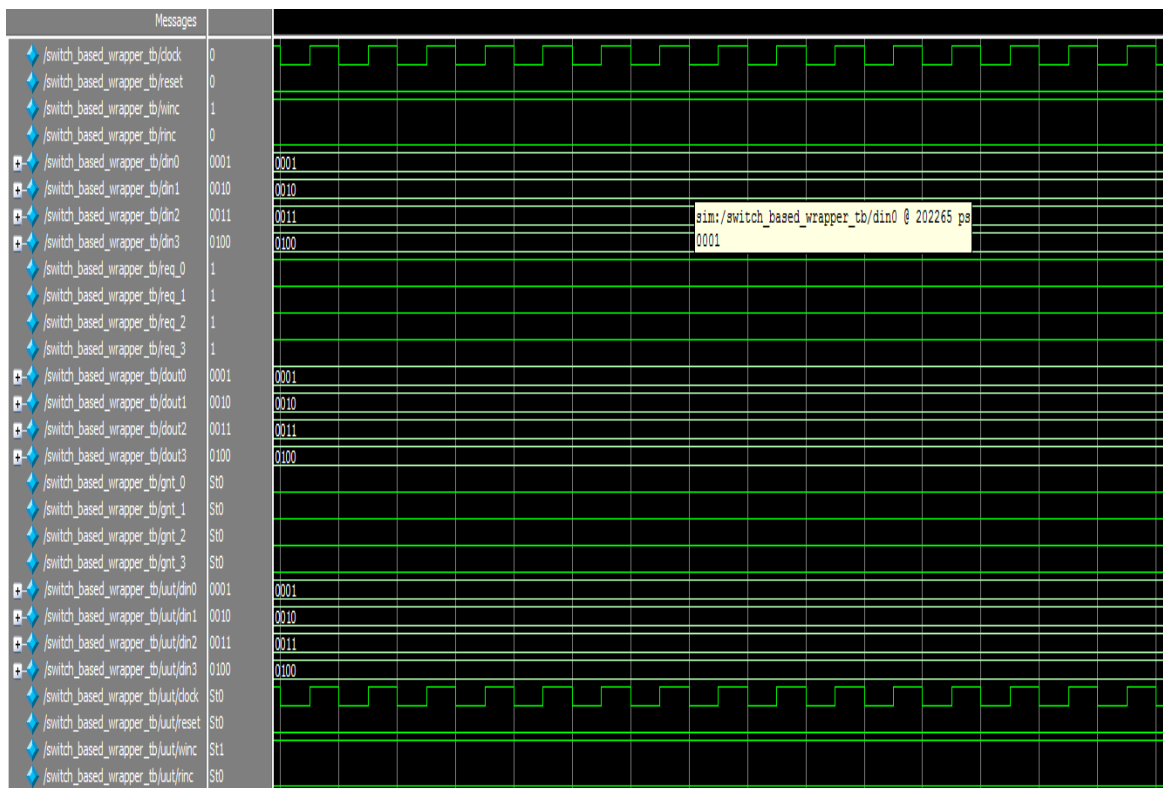## 2. SIMULATION WAVEFORM FOR SWITCH BASED WRAPPER CIRCUIT FOR PROPOSED NETWORK:


Fig 15: shows the simulation waveform for switch based wrapper for proposed network

In figure 15 shows the switch based wrapper circuit simulation waveform in this circuit the input din0 to din3 ,will give the clock and reset , data write and data read will perform the operation will shows the output based request the output will show in the figure.

VIII. FPGA IMPLEMENTATION OF PROPOSED NETWORK
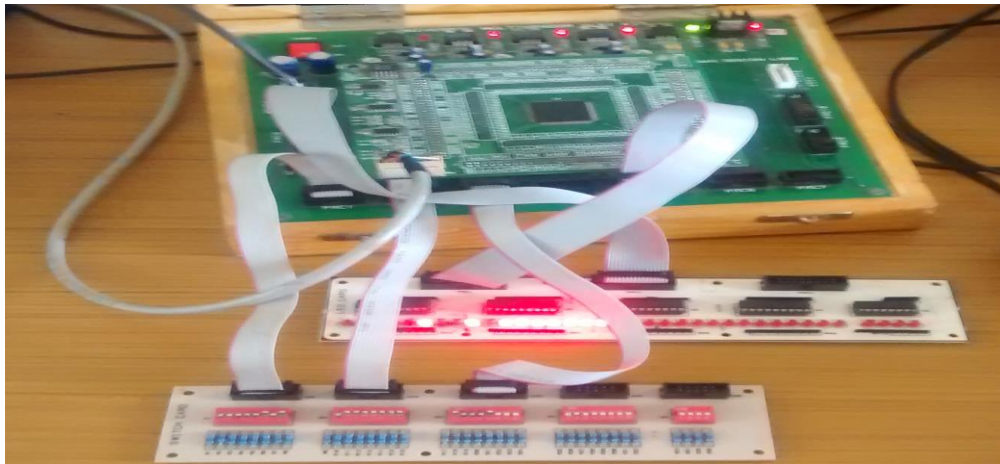
Fig.16: FPGA Implementation of proposed on-chip network

The figure 16 shows the FPGA kit of Spartan 3 family. On this kit implemented the proposed architecture. The output LEDs which are blinked is the output pins of the stage 2 switch and the switches which are enabled acts like Req's, when second switch from left is enabled, ie the Req pin at port of SWO is enabled and data is transferred from source to destination depends the switching data path setup mechanism, here the output is came stage 2 switch 0 at that point data1010. And by Table I gives the synthesis report of architecture according to FPGA. In this FPGA we use device XCS3S400 and package is TQ144 and device speed is -5

TABLE I SYNTHESIS REPORT

Name	Used	Available	Utilization
No of slices	1902	3584	53%
No of slice flip flops	1380	7168	19%
No of 4 input LUTs	3565	7168	49%
Number of bonded IOBs	134	141	95%
Total delay 13.56ns			

TABLE II. COMPARSION WITH OTHER RELATED ON-CHIP NETWORKS

Design	1	2	3	4	5
Number of inputs x outputs	16x16	16x16	16x18	16x18	16x16
Topology	(4,4) 2D Mesh	De Bruijn	Butterfly	Benes 2N-N	3-Stage clos
Data width (bit)	20	20	32	32	16x14
Min/max Latency cycle	NA	NA	5/21	8/22	16/28
Evaluation level	Post -synthesis	Post-synthesis	Post-synthesis	Post-synthesis	Post-silicon
Measured bandwidth	-	-	-	-	28-35
throughput	-	-	-	-	9.061 GHz

As reflected in Table II, due to the heterogeneity of the switching technique, topology, data width, and particularly the evaluation level, it is direct comparison with other related networks. Table II indicates a compact implementation resulting from the proposed approach. Assuming stacking two proposed networks to support a raw 32-bit data of a 16-to-16 permutation,   the proposed network saves area over head compared to butterfly and Benes networks of work.

IX.   CONCLUSION

This paper has presented an on-chip network design supporting traffic permutations in MPSoC applications. By using circuit switching approach combined with path-setup scheme under a clos network topology, the proposed design offers random traffic permutation with compact implementation overhead. Design is implemented using Xilinx ISE 9.1 on FPGA Board of Spartan 3 family, and obtained the synthesis result regarding delay and done power analysis regarding power by that proved that efficiency is improved when compared to existing systems.

ACKNOWLEDGEMENT

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